PETITION DAC IFW

PATENT
P57001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAE-SUNG KIM

Serial No.:	10/766,564	Examiner:	ERDEM, FAZLI
Filed:	29 January 2004	Art Unit:	2826

For: NOVEL CONDUCTIVE ELEMENTS FOR THIN FILM TRANSISTORS USED IN A FLAT PANEL DISPLAY

PETITION UNDER 37 C.F.R. §1.181

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant respectfully petitions from the failure of the Examiner in the Office action issued on 27 July 2005 (Paper No. 0727/2005) to acknowledge the filing and receipt of Applicant's Information Disclosure Statement filed on 12 July 2005 and to consider the references cited therein, and as reasons therefor states that:

Folio: P57001
Date: 8/2/05
I.D.: REB/kf

STATEMENT OF FACTS

1. On 12 July 2005 Applicant filed an Information Disclosure Statement (Paper No. 8) citing twenty four (24) references, and paid $180.00 under 37 C.F.R. §1.17(p). A copy of the foreign patent references cited in the Information Disclosure Statement, namely, JP JP09-153623, JP09-45927 and JP04-265757, was also attached.

2. On 27 July 2005, the Examiner issued an Office action (Paper No. 07242005). In Paper No. 07242005, the Examiner failed to acknowledge the filing and receipt of Applicant's Information Disclosure Statement filed on 12 July 2005, and to confirm the Examiner's consideration of the references cited therein.

REMARKS

A photocopy of a postcard receipt dated 12 July 2005 attesting to the filing of the Information Disclosure Statement (Paper Non. 8), including the PTO-1449 and a copy of the three Japanese references cited therein, as well as a fee of $180.00, is attached to this Petition. A copy of the Information Disclosure Statement filed on 12 July 2005 is also attached.

It is submitted that Applicant's Information Disclosure Statement filed on 12 July 2005 is in full compliance with 37 C.F.R. §§1.97 and 1.98 and, accordingly, the Examiner is respectfully requested to enter the Information Disclosure Statement filed on 12 July 2005 and consider all of the references cited therein.

RELIEF REQUESTED

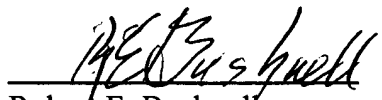
Accordingly, the Commissioner is respectfully requested to direct the Examiner:

A. To enter Applicant's Information Disclosure Statement filed on 12 July 2005;

B. To consider all of the references cited in the Information Disclosure Statement filed on 12 July 2005; and

C. Grant such other and further relief as justice may require.

Respectfully submitted,



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P57001 12 July 2005

Applicant: TAE-SUNG KIM
S.N.: 10/766,564
Filed: 29 January 2004
For: *NOVEL CONDUCTIVE ELEMENTS FOR THIN FILM ....*

Document(s) filed:

1. Information Disclosure Statement & PTO-1449 (Paper No. 8)
2. Copies of JP JP09-153623, JP09-45927 and JP04-265757
3. Check #49346 for $180.00 & Fee Transmittal

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAE-SUNG KIM

Serial No.:	10/766,564	Examiner:	ERDEM, FAZLI
Filed:	29 January 2004	Art Unit:	2826

For: NOVEL CONDUCTIVE ELEMENTS FOR THIN FILM TRANSISTORS USED IN A FLAT PANEL DISPLAY

INFORMATION DISCLOSURE STATEMENT

Paper No. 8

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites, describes and provide copies of the following art references. Under 37 C.F.R. §1.98(a)(2), a copy of U.S. patent reference(s) cited below is not attached.

1. U.S. Patent No. 6,448,612 to Miyazaki *et al.*, entitled *PIXEL THIN FILM TRANSISTOR AND A DRIVER CIRCUIT FOR DRIVING THE PIXEL THIN FILM TRANSISTOR*, issued on September 10, 2002;

2. U.S. Patent No. 6,440,752 to Zhang *et al.*, entitled *ELECTRODE MATERIALS WITH IMPROVED HYDROGEN DEGRADATION RESISTANCE AND FABRICATION METHOD*, issued on August 27, 2002;

3. U.S. Patent No. 6,348,735 to Yamaoka *et al.*, entitled *ELECTRODE FOR SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME*,

issued on February 19, 2002;

4. U.S. Patent No. 6,147,375 to Yamazaki *et al.*, entitled *ACTIVE MATRIX DISPLAY DEVICE*, issued on November 14, 2000;

5. U.S. Patent No. 5,555,112 to Oritsuki *et al.*, entitled *LIQUID CRYSTAL DISPLAY DEVICE HAVING MULTILAYER GATE BUSLINE COMPOSED OF METAL OXIDE AND SEMICONDUCTOR*, issued on September 10, 1996;

6. U.S. Patent No. 5,485,019 to Yamazaki *et al.*, entitled *SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME*, issued on January 16, 1996;

7. U.S. Patent No. 5,345,108 to Kikkawa, entitled *SEMICONDUCTOR DEVICE HAVING MULTI-LAYER ELECTRODE WIRING*, issued on September 6, 1994;

8. U.S. Patent No. 5,243,202 to Mori *et al.*, entitled *THIN-FILM TRANSISTOR AND A LIQUID CRYSTAL MATRIX DISPLAY DEVICE USING THIN-FILM TRANSISTORS OF THIS TYPE*, issued on September 7, 1993; and

9. U.S. Patent No. 4,153,529 to Little *et al.*, entitled *MEANS AND METHOD FOR INDUCING UNIFORM PARALLEL ALIGNMENT OF LIQUID CRYSTAL MATERIAL IN A LIQUID CRYSTAL CELL*, issued on May 8, 1979.

10. U.S. Patent No. 6,147,403 to Matschitsch *et al.*, entitled *SEMICONDUCTOR BODY WITH METALLIZING ON THE BACK SIDE*, issued on November 14, 2000;

11. U.S. Patent No. 6,166,396 to Yamazaki, entitled *SEMICONDUCTOR DEVICES*, issued on December 26, 2000;

12. U.S. Patent No. 4,782,380 to Shankar *et al.*, entitled *MULTILAYER INTERCONNECTION FOR INTEGRATED CIRCUIT STRUCTURE HAVING TWO OR MORE CONDUCTIVE METAL LAYERS*, issued on November 1, 1988;

13. U.S. Patent No. 6,285,123 to Yamada *et al.*, entitled *ELECTRON EMISSION DEVICE WITH SPECIFIC ISLAND-LIKE REGIONS*, issued on September 4, 2001;

14. U.S. Patent No. 5,742,468 to Matsumoto *et al.*, entitled *ELECTRIC CHARGE GENERATOR FOR USE IN AN APPARATUS FOR PRODUCING AN ELECTROSTATIC LATENT IMAGE*, issued on April 21, 1998;

15. U.S. Patent No. 6,271,543 to Ohtani *et al.*, entitled *ACTIVE MATRIX TYPE DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME*, issued on August 7, 2001;

16. U.S. Patent No. 5,278,099 to Maeda, entitled *METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE HAVING WIRING ELECTRODES*, issued on January 11, 1994;

17. U.S. Patent No. 5,345,108 to Kikkawa, entitled *SEMICONDUCTOR DEVICE HAVING MULTI-LAYER ELECTRODE WIRING*, issued on September 6, 1994;

18. U.S. Patent No. 6,414,738 to Fujikawa, entitled *DISPLAY*, issued on July 2, 2002;

19. U.S. Patent No. 6,650,017 to Akamatsu *et al.*, entitled *ELECTRICAL WIRING OF SEMICONDUCTOR DEVICE ENABLING INCREASE IN ELECTROMIGRATION (EM) LIFETIME*, issued on November 18, 2003;

20. U.S. Patent No. 5,607,776 to Mueller *et al.*, entitled *ARTICLE FORMED BY IN-SITU CLEANING A TI TARGET IN A TI+TIN COATING PROCESS*, issued on March 4, 1997;

21. U.S. Patent Publication No. 2003/0222575 to Yamazaki, entitled *LIGHT EMITTING APPARATUS AND METHOD OF FABRICATING THE SAME*, published on December 4, 2003;

22. Japanese Patent Publication No. 09-153623 to Urazono, entitled *THIN FILM SEMICONDUCTOR*, published on June 10, 1997;

23. Japanese Patent Publication No. 09-45927 to Yamazaki, entitled *SEMICONDUCTOR DEVICE*, published on February 14, 1997 (corresponding to U.S. Patent No. 6,166,396 issued on December 26 2000);

24. Japanese Patent Publication No. 04-265757 to Kawasaki, entitled *THIN FILM TYPE THERMAL HEAD*, published on September 21, 1992;

Miyazaki *et al.* '612 discloses "an electronic circuit formed on an insulating substrate and having thin-film transistors (TFTs) comprising semiconductor layers." The thickness of the semiconductor layers is less than 1500 ANG., *e.g.*, between 100 and 750 ANG. A first layer consisting mainly of titanium and nitrogen is formed on the semiconductor layer. A second layer consisting aluminum is formed on top of the first layer.

Zhang *et al.* '752 discloses that "an electrode for use in a ferroelectric device includes a bottom electrode; a ferroelectric layer; and a top electrode formed on the ferroelectric layer and formed of a combination of metals, including a first metal taken from the group of metals consisting of platinum and iridium, and a second metal taken from the group of metals consisting of aluminum and titanium; wherein the top electrode acts as a passivation layer and wherein the top electrode remains conductive following high temperature annealing in a

hydrogen atmosphere."

Yamaoka *et al.* '735 discloses that "an interlayer insulator film 11, a titanium layer 12, a titanium nitride layer 13 that serves as the barrier layer, an aluminum alloy wiring layer 15 and a protective film 18 are formed on top of the silicon substrate 10 to compose the electrode structure."

Yamazaki *et al.* '375 discloses in claim 2 that, "an active matrix display device according to claim 1 wherein at least one of said wiring and said gate electrode comprises a material selected from the group consisting of silicon, aluminum tantalum, titanium, tungsten, molybdenum, an alloy thereof, tantalum nitride, titanium nitride, tungsten nitride and molybdenum nitride."

Oritsuki *et al.* '112 discloses in claim 3 that, "a liquid crystal display substrate according to claim 1, wherein the gate electrode is made of at least one layer made of a material selected from the group consisting of aluminum tantalum and titanium and their alloys."

Yamazaki *et al.* '019 discloses in claim 2 that, "the device of claim 1 wherein said first wiring comprises a material selected from the group consisting of silicon, aluminum, tantalum, titanium, tungsten, molybdenum, an alloy thereof, tantalum nitride, titanium nitride, tungsten silicide, and molybdenum silicide."

Kikkawa '108 discloses"a semiconductor device having an electrode wiring which prevents generation of hillock and has good stress migration capability." A multilayer film includes at least two Al-SI-Cu alloy films and at least two titanium nitride films.

Mori *et al.* '202 discloses "a thin-film transistor comprises a gate electrode formed on

a glass substrate ... the gate electrode is made of titanium-containing aluminum."

Little *et al.* '529 discloses that "electrode surfaces are coated with a passivating material (silicon dioxide, aluminum oxide or titanium dioxide)."

Matschitsch *et al.* '403 discloses novel back side metallizing system which markedly reduces wafer warping of semiconductor wafers without weakening the strength of adhesion to substrate materials. On a silicon semiconductor body an aluminum layer and a diffusion barrier layer that includes titanium are provided. A titanium nitride layer is incorporated into the titanium layer because it has been demonstrated that the titanium nitride layer can compensate for a large proportion of the wafer warping that occurs. Preferably, the usual tempering for improving the ohmic contact between the aluminum layer and the silicon semiconductor body is not performed after the complete metallizing of the semiconductor body, but rather after a first, thin aluminum layer has been deposited onto the silicon semiconductor body.

Yamazaki '396 discloses that in an active matrix liquid crystal display (LCD) device, a conductor line interconnecting a drain of each thin-film transistor and a corresponding pixel electrode constructed with indium tin oxide (ITO) is formed in a three-layer structure in which an aluminum film is sandwiched between a pair of titanium films. This construction prevents poor contact and deterioration of reliability because electrical contact is established between one titanium film and semiconductor and between the other titanium film and ITO. The aluminum film has low resistance which is essential for ensuring high performance especially in large-screen LCDs.

Shankar *et al.* '380 discloses construction of a novel multilayer conductive interconnection for an integrated circuit having more than one conductive layer, comprising a lower barrier layer which may be in contact with an underlying silicon substrate, and comprising

a material selected from the class consisting of TiW and TiN; an intermediate layer of conductive metal such as an aluminum base metal; and an upper barrier layer which may be in contact with a second aluminum base metal layer and which is selected from the class consisting of TiW, TiN, MoSi.sub.x and TaSi where x equals 2 or more.

Yamada *et al.* '123 discloses an electron emission device which includes an electron-supply layer formed of metal or semiconductor; an insulator layer formed on the electron-supply layer; and a thin-film metal electrode formed on the insulator layer, whereby electrons are emitted when an electric field is applied between the electron-supply layer and the thin-film metal electrode. The insulator layer and the thin-film metal electrode have at least one island-like region where the thicknesses of the insulator layer and the thin-film metal electrode gradually decrease.

Matsumoto *et al.* '468 discloses an electric charge generator for use in an apparatus for producing an electrostatic latent image, which includes a plurality of charge generation controlling devices, each charge generation controlling device including: an insulating substrate; a line electrode formed on the insulating substrate; a solid dielectric film formed on the surface of the line electrode; a finger electrode having a hole for generating an electric charge, the hole being formed in the central part of the finger electrode, the finger electrode being formed on the solid dielectric film; a solid insulating film having a hole for passing the electric charge, the hole being formed in the central part of the solid insulating film, the solid insulating film being formed on the finger electrode; and a screen electrode having a hole for ejecting the electric charge, the hole being formed in the central part of the screen electrode, the screen electrode being formed on the surface of the finger electrode via the solid insulating film; wherein the plurality of charge generation controlling devices are arranged on the insulating substrate so as to form the electric charge generator. The solid insulating film is formed of a multilayer solid insulating film including a surface-side layer made of an inorganic insulating film and a

substrate-side layer made of an organic insulating film whereby the durability and the reliability are improved.

Ohtani *et al.* '543 discloses an active matrix type display device having a sufficient auxiliary capacitance and a high aperture ratio. In the device, an auxiliary capacitance (a black mask being in contact with an inorganic layer/the inorganic layer/a pixel electrode being in contact with the inorganic layer) is formed on an interlayer insulating film made of an organic resin film.

Maeda '099 discloses a semiconductor device having a p+ -type silicon source region, an insulating film formed on the source region and having a contact hole, and a wiring electrode connected to the source region through the contact hole. The wiring electrode has a Ti layer formed on the insulating film and an exposed surface of the source region, a TiN layer formed on the Ti layer, and an Al layer formed on the TiN layer.

Kikkawa '108 discloses a semiconductor device having an electrode wiring which prevents generation of hillock and has good stress migration capability. A multi layer film including at least two Al-Si-Cu alloy films and at least two titanium nitride films formed by reactive sputtering laminated alternately with the Al-Si-Cu alloy films has a high mechanical strength against deformation and can effectively prevent generation of hillock. Ti-Al intermetallic compounds are formed in grain boundaries and in interfaces, which is effective to restrict generation of a void. Propagation of a void can be prevented by the intermediate titanium nitride film. Further, the formation of the Ti-Al compounds is restricted and an increase of resistance is negligible.

Fujikawa '738 discloses that, in a display device such as a liquid crystal display device, in order to connect electrodes and wiring with a low resistance, the first titanium nitride film

14 having a hexagonal crystal structure for preventing silicon diffusion is intervened between the drain region 5 composed of a polycrystalline silicon film and the drain electrode 9 composed of an aluminum film. The second titanium nitride film 15 having a hexagonal crystal structure which can be deposited by sputtering with the same target as that for the titanium film 13 and the first titanium film 14 is intervened between the transparent display electrode 12 composed of an ITO film and the drain electrode 9 composed of an aluminum film in order to bring them into ohmic contact. Since the second titanium nitride film 15 is resistant to an etchant for the silicon oxide film and to an etchant for the ITO film, the drain electrode 9 is protected when etching is performed.

Akamatsu *et al.* '017 discloses a method for manufacturing a semiconductor device having on a silicon substrate semiconductor elements and aluminum (Al) alloy wiring leads as electrically connected thereto. The method includes the steps of forming on the silicon substrate an Al alloy layer containing therein copper (Cu), and forming on the Al alloy layer a titanium nitride (TiN) film with enhanced chemical reactivity by using sputtering techniques while applying thereto a DC power of 5.5 W/cm.sup.2 or less. Fabrication of such reactivity-rich TiN film on the Al alloy layer results in a reaction layer of Al and Ti being subdivided into several spaced-apart segments. In this case, the reaction layer hardly serves as any diffusion path; thus, it becomes possible to prevent Cu as contained in the Al alloy layer from attempting to outdiffuse with the reaction layer being as its diffusion path. This makes it possible to suppress or minimize unwanted fabrication of AlN on or above the surface of an Al containing lead pattern, thereby enabling increase in electromigration (EM) lifetime of electrical interconnect leads used.

Mueller *et al.* '776 discloses a novel method of in-situ cleaning a Ti target in a Ti+TiN anti-reflective coating process when such Ti and TiN deposition process are conducted in the same process chamber by the addition of a simple process step and without the use of a shutter.

Yamazaki *et al.* '575 discloses that although an ink jet method known as a method of selectively forming a film of a high molecular species organic compound, can coat to divide an organic compound for emitting three kinds (R, G, B) of light in one step, film forming accuracy is poor, it is difficult to control the method and therefore, uniformity is not achieved and the constitution is liable to disperse. In contrast thereto, according to the invention, a film comprising a high molecular species material is formed over an entire face of a lower electrode connected to a thin film transistor by a coating method and thereafter, the film comprising the high molecular species material is etched by etching by plasma to thereby enable to selectively form a high molecular species material layer. Further, the organic compound layer is constituted by a material for carrying out luminescence of white color or luminescence of single color and combined with a color changing layer or a coloring layer to thereby realize full color formation.

Urazono '623 aims at enabling prevention of voids and hillocks and hence prevention of disconnection without increasing wiring resistance, by providing a multilayer structure of wiring in which an aluminum metal film and a refractory metal film are stacked. English language Abstract is attached.

Yamazaki '927 aims at eliminating contact failures and solve the reliability problems for an active matrix liquid crystal display. English language Abstract is attached.

Kawasaki '757 relates to a thin film type thermal head having high reliability by preventing breaking of wire caused by energizing a power feed layer. English language Abstract is attached.

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a

wide-ranging and thorough search of the relevant art.

A fee of $180.00 is incurred by filing of the Information Disclosure Statement. Applicant's check drawn to the order of Commissioner accompanies this Amendment. Should the check become lost, be deficient in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,

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INFORMATION DISCLOSURE STATEMENT PTO-1449 (PAGE 1 OF 2)	SERIAL NUMBER 10/766,564	DOCKET NO. P57001
	APPLICANT TAE-SUNG KIM	
	FILING DATE 29 January 2004	GROUP 2826

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,448,612	9/02	Miyazaki et al.			
	6,440,752	8/02	Zhang et al.			
	6,348,735	2/02	Yamaoka et al.			
	6,147,375	11/00	Yamazaki et al.			
	5,555,112	9/96	Oritsuki et al.			
	5,485,019	1/96	Yamazaki et al.			
	5,345,108	9/94	Kikkawa			
	5,243,202	9/93	Mori et al.			
	4,153,529	5/79	Little et al.			
	6,147,403	11/00	Matschitsch et al.			
	6,166,396	12/00	Yamazaki			
	4,782,380	11/88	Shankar et al.			
	6,285,123	9/01	Yamada et al.			
	5,742,468	4/98	Matsumoto et al.			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	JP09-153623	6/97	Japan			Abstract	
	JP09-45927	2/97	Japan			Abstract	
	JP04-265757	9/92	Japan			Abstract	

OTHER DOCUMENTS ***(Including Author, Title, Date, Pertinent Pages, etc.)***

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT PTO-1449 (PAGE 2 OF 2)	SERIAL NUMBER 10/766,564	DOCKET NO. P57001
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	6,271,543	8/01	Ohtani et al.			
	5,278,099	1/94	Maedda			
	5,345,108	9/94	Kikkawa			
	6,414,738	7/02	Fujikawa			
	6,650,017	11/03	Akamatsu			
	5,607,776	03/97	Mueller et al.			
	2003/0222575	12/03	Yamazaki			

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